CLAIMS

1. A memory, comprising:

rows and columns of conductors having a memory cell at each intersection thereof; and

a voltage stress circuit for accelerated life testing of a portion of the plurality of memory cells that is coupled to selected memory cells at a predetermined row and selected columns of the memory, the voltage stress circuit comprising a source follower circuit portion to control a stress voltage that is applied across one or more of the portion of the plurality of memory cells, the source follower circuit portion receiving a reference voltage and coupling the stress voltage as a substantially constant voltage to each of the selected memory cells.

2. The memory of claim 1 further comprising:

a mock circuit having one or more mock memory cells implemented on a same integrated circuit as the plurality of memory cells, the mock circuit further comprising:

a source follower transistor coupled to each of the one or more mock memory cells, the source follower transistor being biased by a feedback control signal; and

an operational amplifier having a first input for receiving a stress reference voltage, a second input for receiving a mock stress voltage applied across each of the one or

more mock memory cells by the source follower transistor, and an output coupled to the source follower transistor, the output providing the feedback control signal that also functions as the reference voltage.

3. The memory of claim 2 further comprising:

impedance means coupled between the source follower transistor and each of the one or more mock memory cells, the impedance means duplicating an impedance path within selected portions of the selected columns of the memory.

4. The memory of claim 3 wherein the impedance means further comprises a plurality of select transistors coupled between the source follower transistor and each of the one or more mock memory cells.

5. The memory of claim 2 wherein the stress reference voltage comprises a desired voltage to apply to a tunnel junction of each of the selected memory cells.

6. The memory of claim 2 wherein each of the source follower circuit portion and the source follower transistor further comprise a transistor having a transistor gate oxide that is thicker than gate oxides of transistors implemented in the memory cells to permit higher voltage operation.

7. The memory of claim 1 wherein the plurality of memory cells are magnetoresistive random access memory cells having at least two distinct resistive states and the stress voltage is applied to a magnetic tunnel junction of each of the plurality of memory cells.

8. A method of accelerating life testing of a memory having rows and columns of conductors, the memory having a plurality of memory cells, each memory cell formed at an intersection of a predetermined row and a predetermined column of conductors, comprising:

using a first source follower circuit to generate a constant voltage from a supply voltage that is susceptible to voltage variation;

applying the constant voltage to one or more mock memory columns, each having a mock memory cell;

including within the one or more mock memory columns duplicated impedances that are present in each of the columns of conductors;

comparing with an operational amplifier circuit a voltage across one or more mock memory cells to a stress reference voltage determined to be appropriate for the life testing to provide a reference voltage as an output of the operational amplifier;

coupling the reference voltage as feedback to bias the first source follower circuit;

using the feedback to adjust the voltage across the one or more mock memory cells to a desired value that compensates for a portion of parasitic losses in the memory;

coupling the reference voltage to a second source follower circuit, to generate a stress voltage; and

coupling the stress voltage to a portion of the memory for use in accelerated life testing.

9. The method of claim 8 further comprising:

implementing the plurality of memory cells as magnetoresistive random access memory cells having at least two resistance states.

10. The method of claim 8 further comprising:

coupling the stress voltage to a tunnel junction of each memory cell of the portion of the memory subject to accelerated life testing.

11. The method of claim 8 further comprising:

implementing each of the first source follower circuit and the second source follower circuit with transistors having transistor gate oxides that are thicker than gate oxides of transistors implemented in the memory cells to permit higher voltage operation.

12. The method of claim 8 wherein including duplicated impedances within the one or more mock memory columns further comprise:

coupling one or more transistors between the first source follower circuit and each mock memory cell in the one or more mock memory columns, the one or more transistors duplicating one or more select transistors that are located in the memory between the second source follower and selected memory cells of the plurality of memory cells, the one or more transistors compensating for parasitic effects in the memory.

13. A method of accelerating life testing of a memory having rows and columns of conductors, the memory having a plurality of memory cells, each memory cell formed at an intersection of a predetermined row and a predetermined column of conductors, comprising:

coupling a reference voltage to a first source follower circuit, to generate a stress voltage of substantially constant value that compensates for a portion of parasitic impedances existing within each of the columns of conductors; and

coupling the stress voltage to a portion of the memory for use in accelerated life testing.

14. The method of claim of claim 13 further comprising:

coupling a mock circuit to the memory for generating the reference voltage;

providing a second source follower circuit within the mock circuit to generate a constant voltage;

applying the constant voltage to one or more mock memory columns, each having a mock memory cell;

including within the one or more mock memory columns duplicated impedances that are present in each of the columns of conductors;

comparing with an operational amplifier circuit a voltage across one or more mock memory cells to a stress reference voltage determined to be appropriate for the life testing to provide a reference voltage as an output of the operational amplifier;

coupling the reference voltage as feedback to bias the second source follower circuit; and

using the feedback to adjust the voltage across the one or more mock memory cells to a desired value that compensates for a portion of parasitic losses in the memory.

15. The method of claim 14 further comprising:

implementing each of the first source follower and the second source follower with a transistor having a gate oxide that is thicker than gate oxides of transistors within the plurality of memory cells in the memory.

16. The method of claim 14 wherein including duplicated impedances within the one or more mock memory columns further comprise:

coupling one or more transistors between the second source follower circuit and each mock memory cell in the one or more mock memory columns, the one or more transistors duplicating one or more select transistors that are located in the memory between the first source follower and selected memory cells of the plurality of memory cells, the one or more transistors compensating for parasitic effects in the memory.

17. The method of claim 13 further comprising:

implementing the plurality of memory cells as magnetoresistive random access memory cells having at least two resistance states.

18. The method of claim 13 further comprising:

coupling the stress voltage to a tunnel junction of each memory cell of the portion of the memory that is subject to accelerated life testing.